REMARKS

Claims 1-8 are pending in the application. Claims 1-8 were rejected under 35 U.S.C. §112, second paragraph, as described in paragraph 4 of the Office Action. Claims 1 and 5 were rejected under 35 U.S.C. §102(e), as described in paragraph 6 of the Office Action. Claims 2-4 and 6-8 were rejected under 35 U.S.C. §103(a), as described in paragraph 7 of the Office Action. Claims 1 and 5 are the only independent claims.

The abstract has been amended to be in the form of one paragraph. Accordingly, it is respectfully requested that the objection to the abstract, as discussed in paragraph 2 of the Office Action, be withdrawn.

Attached hereto are replacement formal drawings for Figs. 2, 3, and 9. In particular: the word "INFORMAITON" has been changed to --INFORMATION-- in S206 in Fig. 2; "RECEIVES" has been changed to --READS OUT-- in S304, "RECEIVED" has been changed to --READOUT-- in S305 and S312 has been removed in Fig. 3; and S910 has been removed from Fig. 9.

In light of the replacement formal drawings, it is respectfully requested that the objection to the drawings be withdrawn.

It is respectfully submitted that claims 1-8 have been amended to address the issues raised in paragraph 4 of the Office Action and to comply with 35 U.S.C. § 112, second paragraph without narrowing the scope of the claims as originally presented. Accordingly, it is respectfully requested that the rejection of claims 1-8 under 35 U.S.C. § 112, second paragraph, be withdrawn.

Applicant respectfully submits that claims 1 and 5 are novel over Kawakami within the meaning of 35 U.S.C. § 102(e), for the following reasons.

The data flow controller of independent claim 1 is required to be operable to distribute the data stored in the buffer and to transfer the data in accordance with "**provided transfer conditions**."

Kawakami fails to teach the above identified limitation.

In accordance with the present invention, the data flow controller starts the transfer of data stored in a buffer 120 to separate buffers 141 to 143 on the basis of conditions set by a decoding controller 180 (see paragraph [0030]). Further, the data flow controller sequentially reads out the stored data from the buffer 120, and specifies separate buffers 14i (i = 1 to 3 in an exemplary embodiment) at destinations of transfer in accordance with the set conditions (step S305), and when the readout data has Header 1, for example, the separate buffer 141, which is the destination of transfer of the data, is specified (see paragraph [0032]). Accordingly, the data flow controller is able to distribute data based on a header.

On the other hand, column 5, lines 46-48 of Kawakami describes that the time-divisional multiplexing controller 40 controls the timing of reading out information materials from DMA buffers. Accordingly, the time-divisional multiplexing controller 40 of Kawakami distributes data **based on timing**. As a result, Kawakami is required to solve a problem. In particular, because of time-division multiplexing by the time-divisional multiplexing controller 40, certain data always flows through a MPEG stream bus SB. In other word, as discussed in column 7, lines 19-25 of the reference, data of an information material 14 might even undesirably flow toward a gate controller 32 corresponding to a channel not relating to the current reproduction. Such a problem does not occur in the present invention. In order to solve the problem, the time-divisional multiplexing controller 40 of Kawakami is required to supply effective flags EF to corresponding gate controllers so as to permit only effective information materials (that are desired to be used) to be captured by the corresponding decoder buffers (see col. 7, lines 27-32). The data flow controller of the present application is not required to perform such an operation.

Thus, the data flow controller of the present application does not correspond to the time-divisional multiplexing controller 40 of Kawakami. Accordingly, clearly Kawakami fails to teach a data flow controller that is operable to distribute data stored in the buffer and to transfer the data in accordance with **provided transfer conditions**, as required in independent claim 1.

Independent claim 1 additionally requires a "**separate buffer manager for controlling outputs of said plurality of separate buffers so as to associated with each other in accordance with information for specifying said plurality of separate buffers**."

It is respectfully submitted that Kawakami fails to teach the above identified limitation.

In accordance with the present invention, the separate buffer manager manages separate buffers 141 to 14n (see paragraph [0027]). Accordingly, the separate buffer manager of the present application is able to control **a plurality of separate buffers**. Therefore, the separate buffer manager of the present application is able to control the separate buffers 141 to 14n in mutual association, whereby it is possible to realize synchronized control of video display, audio output, etc.

As for the gate controller 32 of Kawakami, it is clear from Fig. 2 that a separate gate controller 32 is provided for each decoder buffer 34, i.e., there are a plurality of gate controllers 32. Accordingly, it is apparent that each gate controller 32 is able to control only one decoder buffer 34. Since each gate controller 32 is not able to control a plurality of decoder buffers 34 in mutual association, it is not able to realize synchronized control of video display, audio output, etc.

Thus, the separate buffer manger of the present invention does not correspond to the gate controller 32 of Kawakami. Accordingly, Kawakami fails to teach a separate buffer manager operable to control **a plurality of separate buffers**, as required in independent claim 1.

Independent claim 1 additionally requires a decoding controller "**for selecting a separate buffer and a decoder, which are used for the decoding, from among said plurality of separate buffers and said plurality of decoders in accordance with the control information**."

It is respectfully submitted that Kawakami fails to teach the above-identified limitation.

In accordance with the present invention, the decoding controller, having received an instruction, selects three (for example) available decoders from among decoders 151 to 15n. In accordance with an exemplary embodiment, if the decoding controller cannot select a required number of decoders for a decoding process because there is another decoding process which is currently using decoders, the process may wait until all of the required number of decoders are selected, or the process may be started partially in decoders that can be selected (see paragraph [0029]). Accordingly, the decoding controller of the present invention can select available decoders or can be put on standby if a required number of decoders cannot be selected. Therefore, the multiple decoding apparatus of the present invention does not necessarily include a number of decoders which corresponds to the number of channels to be reproduced, whereby it is possible to flexibly and cost effectively configure the multiple decoding apparatus.

Kawakami does not include any description about an element corresponding to the decoding controller of the present application. Accordingly, an information reproduction apparatus of Kawakami necessarily includes a number of decoders 22 correspond to the number of channels to be reproduced. Therefore, Kawakami fails to teach a decoding controller for **selecting** a separate buffer and a decoder **from among a plurality of separate buffers and a plurality of decoders** as required in independent claim 1.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed in a prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the foregoing, it is clear that Kawakami does not anticipate claim 1.

Furthermore, since claims 2-4 are dependent upon claim 1, and therefore include all the limitations thereof, Applicant submits that claims 2-4 additionally are not anticipated by Kawakami.

In view of the above remarks, Applicant respectfully submits that claim 1 is not anticipated by Kawakami, and urge that the rejection of claim 1, and its dependent claims 2-4, under 35 U.S.C. § 102(e), be withdrawn.

Independent claim 5 requires, *inter alia*, "**distributing the data stored in the buffer for each type and respectively storing the data in a plurality of separate buffers**."

It is respectfully submitted that Kawakami fails to teach the above-identified limitation.

The decoder buffer 34 of Kawakami does not distribute data stored in a HDD 20 and a DMA buffer 30 by data type. In Kawakami, the gate controller 32 distributes the data stored in the HDD 20 and the DMA buffer 32.

However, the distributing of claim 5 does not correspond to an operation of the gate controller 32 of Kawakami. In particular, the distributing of claim 5 is performed by the data flow controller. As described above in relation to claim 1, the data flow controller differs from the gate controller 32 of Kawakami. Accordingly, it is clear that Kawakami fails to teach distributing the data stored in the buffer for each type and respectively storing the data in a plurality of separate buffers, as required in independent claim 5.

In light of *Akzo*, it is respectfully submitted that claim 5 is novel over Kawakami within the meaning of 35 U.S.C. § 102.

It is respectfully submitted that claims 1-8 are patentable over the prior art of record within the meaning of 35 U.S.C. § 103. In particular, Haskell et al. (Haskell) fails to teach the shortcomings of Kawakami such that a combination of the teachings of Kawakami and Haskell would teach that which is required in independent claims 1 and 5.

As discussed in page 7 of the Office Action, Haskell is relied upon for allegedly disclosing:

> "a buffer control for variable bit rate channel as shown in Figures 1-4, and teaches the conventional notification of overflow situations associated with encoder and decoder buffers (see column 17, line 66 to column 18, line 13), and the particular termination of packets of data within the decoder as one way of preventing overflow in the buffers, thereby stopping decoding to the decoder, data extraction, data transfer to the specific buffer, and discarding data directed toward the specific buffer (see column 16, lines 27-39)."

Contrary to that discussed in the Office Action, Haskell fails to teach stopping decoding to a decoder, stopping data extraction and discarding data directed toward specific buffer as required in claims 2-4. In particular, column 16, lines 27-39 of Haskell merely describes that a current packet is terminated in order to prevent overflow of buffers.

In any event, it is respectfully submitted that Haskell fails to teach: a data flow controller operable to distribute a data stored in a buffer and to transfer the data in accordance with provided transfer conditions, a separate buffer manager for controlling outputs of a plurality of separate buffers so as to associated with each other in accordance with information for specifying the plurality of separate buffers or a decoding controller for selecting a separate buffer and a decoder, which are used for the decoding, from among the plurality of separate buffers and the plurality of decoders in accordance with the control information, as required in independent claim 1; or distributing the data stored in the buffer for each type and respectively storing the data in a plurality of separate buffers, as required in independent claim 5. Because neither Kawakami nor Haskell teach that which is required in independent claims 1 and 5, it is respectfully submitted that a combination of the teachings of Kawakami in view of Haskell additionally fails to teach that which is required in independent claims 1 and 5.

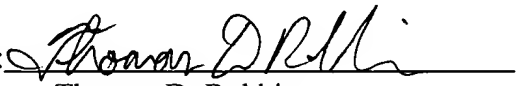
In light of the above discussion, it is respectfully submitted that independent claims 1 and 5 are patentable over the combination of the teachings of Kawakami in view of Haskell within the meaning of 35 U.S.C. § 103. Further, as claims 2-4 and 6-8 are dependent upon claims 1 and 5, respectively, and therefore include all of the limitations thereof, it is additionally respectfully submitted that claims 2-4 and 6-8 are patentable over a combination of Kawakami in view Haskell within the meaning of 35 U.S.C. § 103.

Having fully and completely responded to the Office Action, Applicant submits that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

Respectfully submitted,

Akira KAMIYA

By: 

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